ADVANCED MATERIALS TECHNOLOGIES
www.advmattechnol.de

Hybrid Tuning of Sub-Filaments to Improve Analog Switching Performance in Memristive Devices

*Pan Hu, Sushmit Hossain, Zerui Liu, Deming Meng, Yunxiang Wang, Tse-Hsien Ou, Hao Yang, Buyun Chen, Zhi Cai, Yudi Shi, Mark Barnell, Qing Wu, Stephen B. Cronin, and Wei Wu**

Memristive devices are promising candidates for analog computing applications such as neuromorphic computation. Larger dynamic ranges and more sufficient multilevel states can enable the significant development of memristor-based utilizations. Herein, a method to improve the analog switching performance of memristors through a hybrid tuning (coarse and fine tuning) of two sub-filaments is demonstrated. The creation of sub-filaments inside the dielectric switching layer is realized by deploying Pt metal islands in the switching layer. Given the different material stack configurations of the two sub-filaments, they exhibit different switching properties to play the roles of coarse and fine tuning respectively in the memristor. Based on the above mechanism, a Pt/Ta/Al_2O_3/Pt island/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor is proposed and fabricated. Through the hybrid tuning of two sub-filaments, a combined dynamic range of 600 Ω to 50 kΩ is achieved. Compared to the reference Pt/Ta/Al_2O_3/Pt memristors (dynamic range: 600 Ω to 8 kΩ), both dynamic range and multilevel resistance states are increased significantly. Meanwhile, the energy efficiency is improved because the resistance of tunable states can be set to larger values. Furthermore, this mechanism can be incorporated into various existing memristors to improve their dynamic range and multilevel states, which extensively enriches the applications of memristors.

1. Introduction

Memristive devices with continuously tunable resistance states possess tremendous potential for analog computing applications such as neuromorphic computing because the internal resistance states of memristors can be adaptively changed to emulate the biological synapses.[1–8] It is generally accepted that the progressive resistance tuning of memristors is associated with the charged dopants in the switching layer, oxygen deficiency (n-type), oxygen excess (p-type), and metal cations can serve as dopants in the memristors.[9–14] Under the external stimulus such as voltage and current, the directional motion of dopants causes internal resistive switching due to the chemical and phase changes within the switching layer.[15–18] Once a large enough bias is applied, a conductive dopant channel can be formed inside the switching layer and this channel is usually called filament which has tens or hundreds of nanometers in diameter.[19–21]

With the development of memristor-based analog computing, there is an increasing demand for memristors with wide dynamic ranges and large amounts of multilevel states because they offer more programable states.[22–26] The memristors can be tuned to multiple resistance states by manipulating the maximum applied voltage and current; the total number of tunable

P. Hu, S. Hossain, Z. Liu, D. Meng, Y. Wang, T.-H. Ou, H. Yang, B. Chen, Y. Shi, S. B. Cronin, W. Wu
Ming Hsieh Department of Electrical and Computer Engineering
University of Southern California
Los Angeles, CA 90089, USA
E-mail: wu.w@usc.edu

Z. Cai
Mork Family Department of Chemical Engineering & Materials Science
University of Southern California
Los Angeles, CA 90089, USA

M. Barnell, Q. Wu
Air Force Research Laboratory
Information Directorate
Rome, NY 13441, USA

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/admt.202300109

DOI: 10.1002/admt.202300109

states heavily depends on the dynamic range.[27] Given a limited dynamic range, the number of multilevel resistance states is difficult to be enhanced.[28] Meanwhile, even a large dynamic range does not always lead to more multilevel states since a huge resistance jump may happen between two neighboring states.[29] The incomplete understanding of the complex switching mechanisms also obstructs the relevant studies. Many methods have been implemented, such as doping or adding different metal oxide films into the memristors, while the improvement is still restricted.[8,30,31]

In this work, we report a new method to improve the analog switching performance of memristors through a hybrid tuning of two sub-filaments. One sub-filament takes charge of a coarse resistance adjustment, and the other is responsible for a fine adjustment. The two sub-filaments are created by deploying Pt metal islands inside the oxide switching layer. Because of a stronger electric field strength near Pt islands under applied bias, the dopant ions tend to move toward the metal islands. A complete filament is then cut into two sub-filamentary sections by the islands. By selecting appropriate material stacks and thicknesses, two sub-filaments exhibit different switching behavior to play diverse roles (coarse and fine tuning). To experimentally demonstrate the above mechanism, Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristors with Pt islands and ultra-thin Ti layer were fabricated and characterized. This thin Ti layer is used to provide extra dopants to lower the required voltage and current for the switching process. The hybrid tuning of two sub-filaments results in a dynamic range from 600 Ω to 50 kΩ, such range is significantly broader than the dynamic range (600 Ω – 8 kΩ) of a reference Pt/Ta/Al_2O_3/Pt memristor without sub-filaments. It is noteworthy that large numbers of multilevel conduction states are uniformly distributed within this broad dynamic range. More importantly, the mechanism of creating sub-filaments is compatible with existing memristors, it can provide guidance for the future research on large dynamic range and energy-efficient memristors.

2. Theoretical Demonstration of Dynamic Range Improvement by Sub-Filaments

For a conceptual explanation of how the insertion of metal islands improves the dynamic range of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristors, a schematic of sub-filaments structure is shown in **Figure 1**a. Based on a Pt/Ta/Al_2O_3/Pt memristor, ultra-thin Pt and Ti layers are deposited inside the Al_2O_3 switching layer to form a Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt structure. Pt acts as metal islands to divide each filament into two sub-filaments,[32] and Ti provides extra dopants for the switching process (more details of Pt and Ti roles are discussed in Results and Discussion section). Pt island stays in the middle of the switching layer and blocks the diffusion of dopants across it. Then two sub-filamentary sections are formed and separated by the Pt island, the island can be regarded as the bottom electrode of the upper sub-filament as well as the top electrode of the lower sub-filament. Therefore, the entire memristor can be assumed as a series connection of two individual sub-memristors. The upper sub-memristor has an identical material stack to Pt/Ta/Al_2O_3/Pt memristors, the electrical characterization of Pt/Ta/Al_2O_3/Pt memristors indicates that continuously tunable states can be achieved in the device. Simultaneously, due to a different material stack of the lower Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt sub-memristor, it behaves diversely from the upper sub-memristor. Only two states, high and low resistance states, were experimentally observed without any intermediate tunable states in the control Pt/TiO_x/Al_2O_{3-x}/Pt memristors. In this case, the upper sub-filament works as a fine adjustment for the resistance of the entire memristor and the lower sub-filament is responsible for a coarse adjustment (More details of electrical characteristics of upper and lower sub-memristors are given in the Results and Discussion section). Compared to the initial Pt/Ta/Al_2O_3/Pt memristor without metal islands, the entire dynamic range of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristors is enlarged because of the hybrid tuning of two sub-filaments.

However, there is considerable uncertainty in the forming locations of filament, not to mention that the metal islands are also deposited at random positions. While in our design, metal island must be exactly located in the path of a filament to divide it into two sections. A Comsol Multiphysics simulation was performed to validate that the filament tends to explicitly situate at the locations of metal islands. As shown in Figure 1b, when there is a Pt island existing in the Al_2O_3 switching layer under applied bias (1 V), the electric field strength becomes stronger near the top and bottom of the island. The resistive switching process of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristors is mainly driven by electric field, which is verified by its bipolar switching behavior in the electrical characterization.[33] Meanwhile, the drift process of dopants has been proved to be primarily affected by the electric field before the completion of filament formation.[34] Hence, the dopants have the tendency to aggregate near the metal island and compose a filamentary channel there under applied bias.

3. Results and Discussion

3.1. Hybrid Tuning of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt Memristor

The fabrication approach of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristors is shown in Figure S1a–d (Supporting Information). Al_2O_3 in the switching layer was grown at 80 °C using atomic-layer deposition (ALD) that is able to control film thickness at atomic precision.[35,36] One nanometer Pt and 2 nm Ti layers inside the switching layer were deposited by electron-beam metal evaporator. Here 1 nm Pt is ultra-thin and this layer can hardly been characterized by scanning electron microscope (SEM) due to the limited contrast of SEM. Instead, 3 nm Pt was deposited on Si substrate for SEM characterization and the corresponding SEM image is shown in Figure S1f (Supporting Information). Discontinuous film topography is captured on 3 nm Pt layer, hence 1 nm Pt is in island form and such observation also matches other published work.[32,37] The typical I–V curves of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor are shown in **Figure 2**a,b. Different from normal memristive devices that only exhibit a single relation between voltage and current, two separate resistance tuning ranges can be observed on each Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor. One I–V curve is corresponding to the tuning range

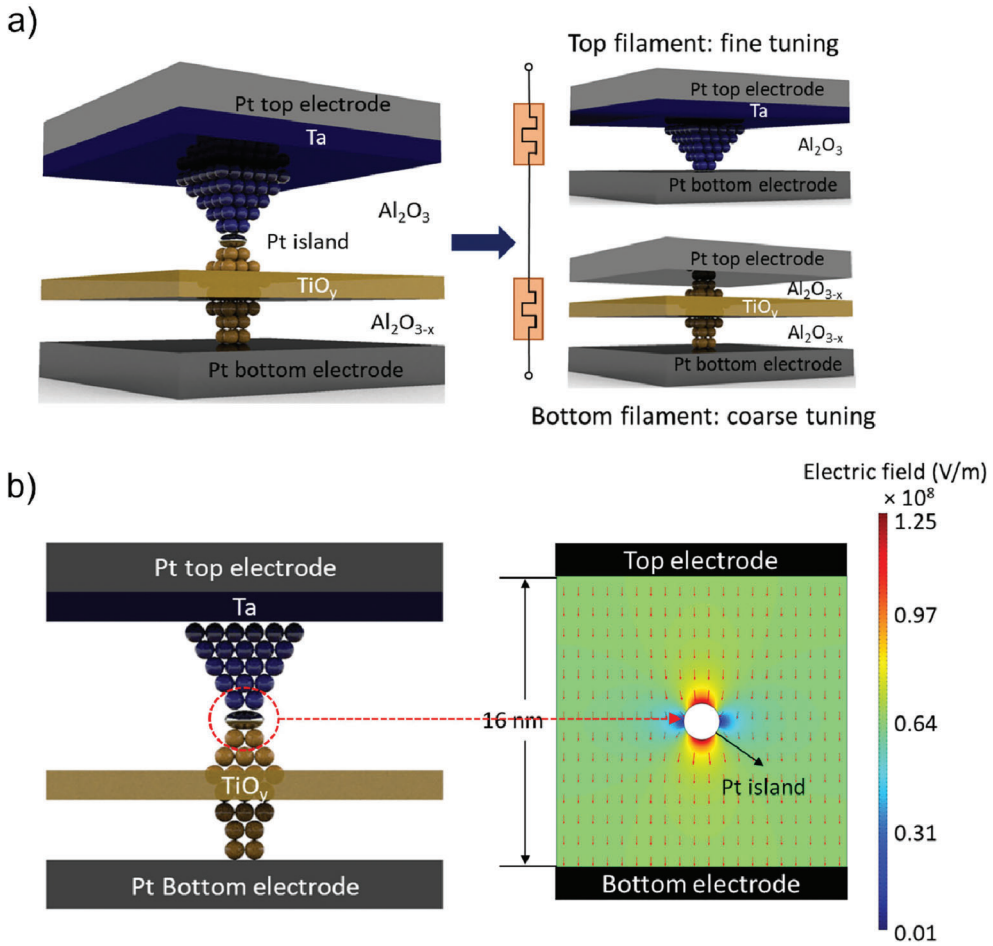

Figure 1. Schematic of hybrid tuning of sub-filaments. a) Schematic of sub-filaments in Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor. Two sub-filaments are divided by Pt islands and the whole memristor can be considered as a series connection of two sub-memristors. b) Simulation of Electric field distribution in Al_2O_3 switching layer when there is a spherical Pt island (2 nm diameter) inside. Electric field is stronger near the Pt island and the dopants inside the switching layer tend to move towards the island.

under relatively low device resistance (Figure 2a), while the other happens when the device is maintained at higher resistance (Figure 2b). Here low resistance dynamic range (LRDR) and high resistance dynamic range (HRDR) are used to distinguish these two distinct switching performances. The orange curve in Figure 2a shows the *I*–*V* curve under LRDR (600 Ω to 19 kΩ), in which the applied RESET bias should be controlled less than −2 V. In particular, the lower sub-filament is kept at low resistance state because its RESET threshold voltage is not reached. After applying a higher RESET bias (blue curve), the device can be switched to a higher resistance (50 kΩ) state when the lower sub-filament is reset as shown in Figure 2c. As this time, if the compliance current (highest current limit) of SET process is controlled correctly (≤2 mA), the resistance of the device is merely switched to 19 kΩ instead of 600 Ω by the reason that the lower sub-filament requires larger voltage and compliance current to be set to low resistance state. Consequently, the device can stay within HRDR (19–50 kΩ) as shown in Figure 2b. Once larger voltage and compliance current are applied (orange curve), the memristor can jump from HRDR back to LRDR because the lower sub-filament is turned into low resistance state as shown in Figure 2d. Depending on the required resistance range, each memristor can be switched repeatedly between HRDR and LRDR. While the resistance change is not continuous between HRDR and LRDR because of the large resistance shift caused by the switching of lower sub-filament. More explanations of the resistance tuning discontinuity can be found in Section 3.4. To investigate the multilevel states within HRDR and LRDR, current pulses (130 ms) were used to tune the memristor to various resistance states. The memristor was switched to either HRDR or LRDR first and then the multilevel states were measured within the corresponding dynamic range. As shown in Figure 2e, a large amount of multilevel resistance states can be obtained in both HRDR (blue curves) and LRDR (orange curves). Under negative voltage sweeps (0 to −0.1 V), Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor shows linear *I*–*V* curves at different conductance states as well (Figure S2a, Supporting Information). The corresponding resistance tuning characteristics are provided in Figure 2f, two separate tuning curves coexist in a single memristor because of the unique HRDR and LRDR, the overall resistance tuning range is from 600 Ω to 50 kΩ.

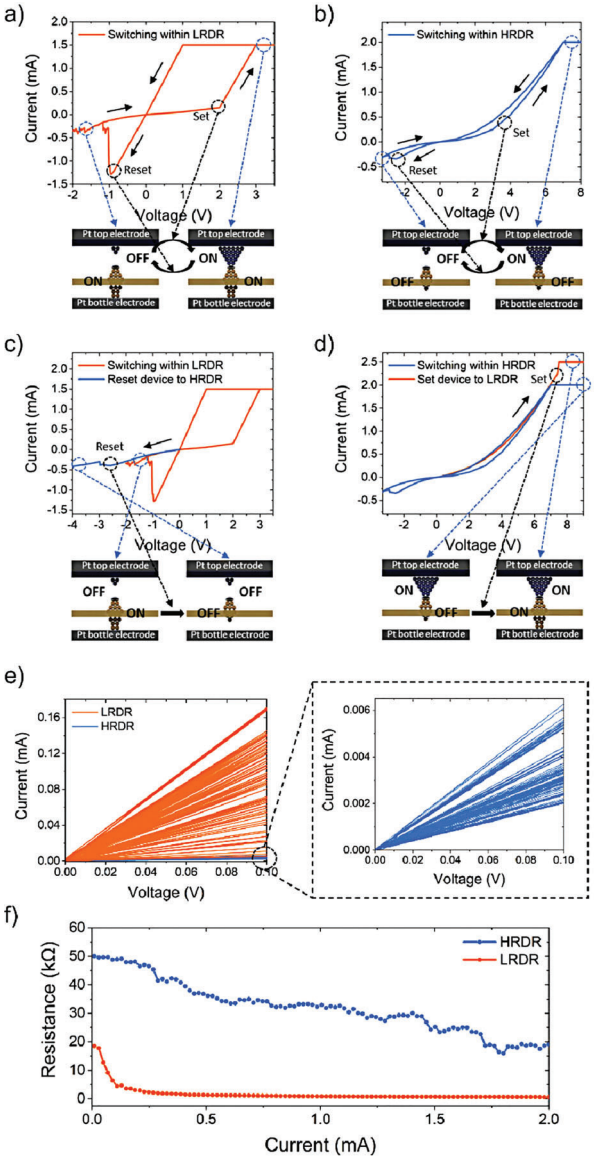

Figure 2. Hybrid tuning of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor. a) *I–V* characteristics of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor within LRDR. The corresponding dynamic range is 600 Ω to 19 kΩ. b) *I–V* characteristics of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor within HRDR. The corresponding dynamic range is 19–50 kΩ. c) Switching from LRDR to HRDR by applying a higher negative voltage (blue curve). d) Switching from LRDR to HRDR by applying higher positive current and voltage (orange curve). e) Multilevel states within LRDR (orange lines) and HRDR (blue lines). f) Relation between resistance and programming current of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor within LRDR (orange curve) and HRDR (blue curve).

3.2. Analog Performances of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt Memristor

As discussed above, the conductance tuning range of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor ranges from 20 to 2000 μS. To study the number of programmable states, Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor was set to different conductance states (**Figure 3**a) and the standard deviation of tuning the memristor to an exact conductance state is 0.89 μS. As a result, the number of programmable states in Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor is 1112 states. As shown in Figure 3b, compared to Pt/Ta/Al_2O_3/Pt memristor without Pt islands in the switching layer, the number of conductance states of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor is enhanced from 157 states to 1112 states because of its extra conductance tunable range. The significant improvement of programmable conductance states can be attributed to the increased dynamic range as well as the higher state density when the device is within the high resistance tuning range. Although continuously tunable states are confirmed on Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor, these conductance states are required to be stable enough for practical analog computing applications.[38] The retention test of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor is shown in Figure 3c. The device is programmed to various conductance states and then reading pulses are applied on the device every 10 s to record the conductance value of the device. The device keeps good stability within at least 1200 s and the conductance variation is always <5 μS. Different from the switching endurance tests of normal memristors that only demonstrate the switching between low conductance state (LCS) and high conductance state (HCS), the switching endurance of a middle conductance state (MCS) is uniquely provided for Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor because the sub-filament switching of the device results in an extra conductance state between the switching of HRDR and LRDR. In the endurance test, Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor can be switched reliably at least 300 cycles among the three different conductance states as shown in Figure 3d. Figure 3e shows the analog programming process of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor under voltage pulses with 0.7 V amplitude and 500 ns width. The memristor is initially set to 2.82 kΩ within LRDR and a single 500 ns pulse is enough to program the device to another state (2.17 kΩ), the device will keep stable in a final state (1.95 kΩ) after 2 voltage pulses and the following pulses will not affect the state anymore. To demonstrate that the memristor can have even faster programming speed, 1 V voltage pulse with 100 ns width was applied on Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor. The experimental result can be found in Figure S2b (Supporting Information). Due to the slow sampling rate of the measurement setup, the resultant pulse shape slightly deformed. While the memristor exhibits obvious resistance shift (5.38–0.88 kΩ) after applying one single pulse, such observation confirms that Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor can respond to a voltage pulse with less than 500 ns width and large resistance change can be induced by one single voltage pulse. Meanwhile, the switching energy consumption is merely 257 pJ. The switching energy consumption can be even smaller if a narrower width pulse is adopted for the programming.

3.3. Engineering of Sub-Filaments

Creating sub-filaments can be realized by the deployment of Pt metal islands in the switching layer, and different sizes of Pt

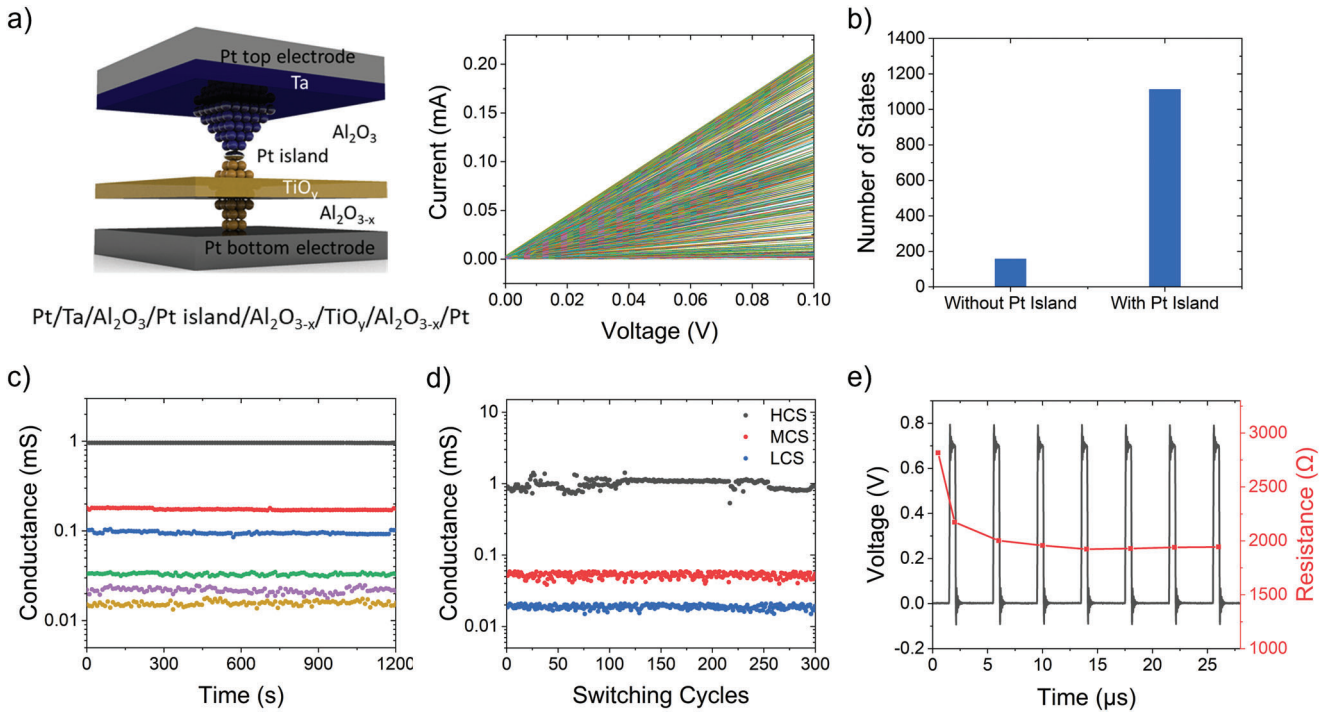

Figure 3. Analog Performances of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt Memristor. a) Multilevel conductance states of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt Memristor. b) Comparison of multilevel conductance states between memristors with and without Pt islands. The number of conductance states of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor is enhanced from 157 states to 1112 states. c) The retention test of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor within 1200 s. d) Switching endurance test of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor during 300 cycles. e) Analog programming of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor under voltage pulses. Pulse amplitude is 0.7 V and width is 500 ns.

islands may lead to diverse device performances. To demonstrate the size effect of Pt island, Comsol simulation was performed as shown in Figure S3a (Supporting Information). Compared to the spherical Pt island with 2 nm diameter in Figure 1b, the lateral dimension of Pt island in Figure S3a (Supporting Information) is increased to 8 nm while the vertical dimension is kept at 3 nm to indicate the curvature change due to aggregation of individual islands. The calculated strongest electric field strength is 0.89 $\times 10^8$ V m^{-1} and this value is smaller than the calculated field strength (1.25×10^8 V m^{-1}) of the spherical island case. Therefore, the electric force applied on the charged dopants becomes weaker when thicker Pt layer is deposited and it tends to form a film. Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor with 2 nm deposited Pt was fabricated to study the size effect of Pt islands and its *I–V* curves are shown in Figure S3b (Supporting Information). This device requires high voltage and current for the switching process and such observation is corresponding to the fact that induced electric field is weaker in the switching layer. As a result, higher voltage and current are required for the switching.

A Thin TiO_y layer is used to lower the required switching voltage and current for SET and RESET processes through offering more dopants for the switching process. Pt/Ta/Al_2O_3/Pt/Al_2O_3/Pt memristors with 1 nm Pt layer were the initial design to achieve sub-filamentary sections in the switching layer. Pt was selected due to its inert properties that avoid the unexpected reactions in the switching layer.[39] However, the required switching voltage and current of Pt/Ta/Al_2O_3/Pt/Al_2O_3/Pt memristors are high enough to induce the electrical breakdown. The required voltages for electroforming and following RESET process can be found in **Table 1**, each value is calculated based on an average value of ten devices. 12.78 V had to be enforced to completely electroform the devices, which made the devices easy to break down during the switching cycles. Considering the fact that the dopants prefer moving towards metal islands due to a stronger electric field there, and the existence of Pt islands obstructs the diffusion of dopants to affect the switching of the Pt island/Al_2O_3/Pt bottom electrode part. As a result, large voltage and current are necessary for the switching process of the memristors but such large voltage and current result in the compromise of device reliability. Typical electroforming and RESET I-V curves of Pt/Ta/Al_2O_3/Pt/Al_2O_3/Pt memristors are shown in Figure S4a (Supporting Information).

Ti is known as an oxygen-reactive metal and it can enrich the dopant density for switching process,[40,41] and hence lower the switching and electroforming voltages of the memristors. To demonstrate this, Pt/Ta/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristors with different thickness Ti layers were then fabricated and tested. The resistances of all control memristors after the electroforming-RESET cycle are summarized in Table 1 to act as dopant density indicators. It can be clearly seen that the memristors without Ti layer have resistances large than 10^3 kΩ after electroforming-RESET cycle, low dopant densities can be expected in these memristors. However, the

Table 1. Electroforming and RESET Characteristics of Control Memristors.

Memristor Structure	Switching Layer	Electroforming Voltage [V]	RESET Voltage [V]	Resistance after Electroforming-RESET
$Pt/Ta/Al_2O_3/Pt/Al_2O_3/Pt$	$Al_2O_3/Pt/Al_2O_3$ (8 nm/ 1 nm/ 8 nm)	12.78	−2.77	$>10^3$ kΩ
$Pt/Ta/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt$	$Al_2O_{3-x}/TiO_y/Al_2O_{3-x}$ (8 nm/ 1 nm/ 8 nm)	7.54	−2.03	483 kΩ
	$Al_2O_{3-x}/TiO_y/Al_2O_{3-x}$ (8 nm/ 2 nm/ 8 nm)	5.71	−2.21	31 kΩ
	$Al_2O_{3-x}/TiO_y/Al_2O_{3-x}$ (8 nm/ 4 nm/ 8 nm)	4.97	−2.18	6 kΩ
$Pt/Ta/Al_2O_3/Pt$	Al_2O_3 (8 nm)	3.6	−1.83	$>10^3$ kΩ
	Al_2O_3 (16 nm)	5.93	−1.93	$>10^3$ kΩ

presence of Ti in the switching layer significantly reduces the resistance of $Pt/Ta/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt$ memristors after the electroforming-RESET cycle (more information can be found in Figure S4b,c (Supporting Information). Given the potential transition of Ti to its sub-oxidation states TiO_x during the device fabrication process and electroforming process, the emergence of more dopants in the memristors can be reasonably explained. Near the Ti-rich region, the Ti sub-oxides are more stable than Al_2O_3, it is possible for Ti to grab oxygen ions from Al_2O_3 near the Ti-rich region.[42,43] Furthermore, the formation Gibbs free energy of possible Ti sub-oxides such as Ti_2O_3 is very close to or even lower than Al_2O_3 of −1582.3 kJ mol^{-1}, the oxidation of Ti is thermodynamically favorable in the switching layer.[44] When oxygen vacancies (dopants) are formed, conduction electrons are simultaneously released in order to maintain the total charge balance.[19] Also, high resistance was observed on 2 nm Ti film after deposition which confirmed its oxidation to Ti sub-oxides TiO_y. Different from Ti, Pt is known as an inert metal. The introduction of Pt should impose negligible influence on the dopant density. This is confirmed by the similar resistance between $Pt/Ta/Al_2O_3/Pt/Al_2O_3/Pt$ memristors and $Pt/Ta/Al_2O_3/Pt$ memristors (Table 1) after the electroforming-RESET cycle. In conclusion, oxygen-reactive Ti and inert Pt behave differently inside $Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt$ memristors. Ti assists in the production of additional dopants to lower the switching voltage and current, while Pt is aimed to create sub-filaments.

3.4. Sub-Memristors for Coarse and Fine Resistance Tuning

$Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt$ memristor can be roughly considered as a combination of two sub-memristors separated by Pt islands as shown in **Figure 4**a. Although the switching characteristics of this combination may not be completely identical to the actual device, the study on sub-memristors can still provide valuable information to identify their different roles in the switching process. Therefore, we fabricated $Pt/Ta/Al_2O_3/Pt$ and $Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt$ memristors to study the characteristics of each sub-filaments. The upper sub-filament possesses a $Pt/Ta/Al_2O_3/Pt$ stack, which is also the initial memristor architecture without metal islands. Nevertheless, such sub-memristor has a shorter filament length defined by the thickness of Al_2O_3 switching layer. To study the effect of Al_2O_3 thickness on the final device performance, two different Al_2O_3 thicknesses 8 nm and 16 nm were selected, because Al_2O_3 thickness less than 8 nm makes the switching process of memristors unstable (memristors are initially ON without electroforming). A higher voltage is demanded for the electroforming of 16 nm Al_2O_3 memristors compared to 8 nm Al_2O_3 devices, and similar RESET voltages are observed on both memristors as shown in Table 1. Their *I–V* curves after multiple switching processes are shown in Figure 4b respectively, the results indicate that two memristors have similar electrical characteristics after several SET-RESET cycles. It is noticeable that the variation of Al_2O_3 thicknesses in $Pt/Ta/Al_2O_3/Pt$ memristors results in a negligible change on the final resistance tuning behavior, both devices have comparable dynamic ranges between 600 Ω and 8 kΩ as shown in Figure 4b insert figure. Therefore, $Pt/Ta/Al_2O_3/Pt$ memristors with different Al_2O_3 thicknesses are confirmed to have continuously tunable resistance states, the resistance of upper sub-filament can be adjusted finely.

As mentioned earlier, the lower part of a $Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt$ memristor can be approximately regarded as a $Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt$ sub-memristor with 2 nm Ti in the switching layer. In our experiments, $Pt/TiO_x/Al_2O_{3-x}/Pt$ memristors were fabricated to estimate the performance of lower sub-filaments instead of $Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt$ memristors because Pt electrode has poor adhesion to Al_2O_3 layer. Figure 4c shows the corresponding *I–V* curves of electroforming and following RESET processes, the device can be hardly electroformed (average 7.81 V calculated from 10 memristors). Moreover, the memristor is difficult to be switched OFF (average −8.93 V calculated from 10 memristors). No consecutively tunable resistance states could be achieved, only high resistance and low resistance states were observed on this memristor. In this case, the lower sub-filament should be responsible for a coarse resistance adjustment of the entire device.

3.5. Validation of Sub-Filaments Coexistence

Although unique resistance tuning behavior of $Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt$ memristors can be reasonably explained by the coarse and fine adjustments of sub-filaments, more evidences are required to prove the existence of sub-filaments. Through the study on the evolution of filament formation during the switching process, valuable information can be acquired to validate the coexistence of two sub-filaments divided by Pt islands. During the electroforming and following SET processes, gradually increasing current pulses (130 ms) were applied on the memristor to induce the switching of internal states. Every time after enforcing an increased current pulse, the

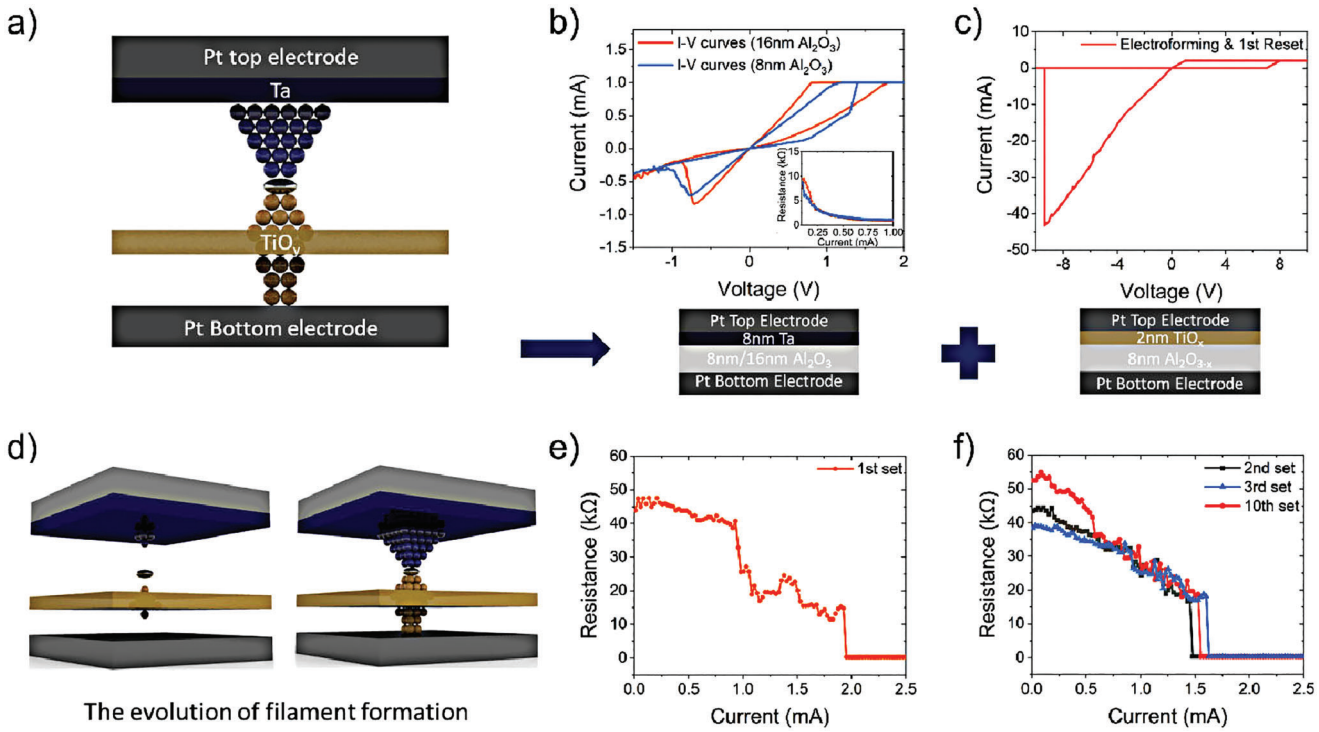

Figure 4. Electrical characteristics of sub-memristors and Resistance evolution of sub-filaments formation. a) Structure of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor. It can be considered as a combination of two sub-memristors separated by Pt islands. b) *I–V* characteristics of Pt/Ta/Al_2O_3/Pt sub-memristors with different Al_2O_3 thicknesses. The memristor requires relatively low voltage and current for switching. The insert figure is the resistance tuning characteristics of Pt/Ta/Al_2O_3/Pt memristors with different Al_2O_3 thicknesses. c) *I–V* characteristics of Pt/TiO_x/Al_2O_{3-x}/Pt sub-memristor. The memristor requires high voltage and current for switching, no consecutively tunable resistance states can be observed on it. d) The evolution of filament formation. The formation details can be studied by recording the resistance of SET process. e) First SET processes of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor after electroforming. Two abrupt resistance drops can be observed. f) Following SET processes of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristor. With more SET-RESET cycles, the first abrupt resistance transition becomes smoother.

corresponding device resistance was measured to record the current situation of filament because resistance values of memristors are strongly related to the inner filament morphology.[45] The resistance evolution of Pt/Ta/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt and Pt/Ta/Al_2O_3/Pt memristors can be found in Figure S5 (Supporting Information). In the first SET process after electroforming, only one abrupt resistance transition is encountered in both Pt/Ta/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt and Pt/Ta/Al_2O_3/Pt memristors, which indicates the formation of one single filament in the switching layer.

Unlike above two types of memristors, the resistance evolution of Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristors reveals interesting phenomena as shown in Figure 4d. After electroforming, the device is reset to a resistance around 45 kΩ. In the following first SET process, the device resistance is kept ≈45 kΩ for a moment and then reduced to 20 kΩ in a sudden transition under 1 mA current (Figure 4e). A second abrupt drop in resistance happens when the current is larger than 1.9 mA. There are totally two fast resistance drops occurring in the first SET process. Given the fact that only one sudden resistance shift is detected in Pt/Ta/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt and Pt/Ta/Al_2O_3/Pt memristors, the presence of extra resistance drop implies the existence of extra sub-filamentary section in Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristors. Remember that the only structural difference between Pt/Ta/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt and Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristors is the extra 1 nm Pt layer, the incorporation of this Pt layer introduces one more resistance drop for the Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristors. Thus, it is reasonable to conclude that the two sub-filaments are separated by Pt islands rather than Ti layer.

Moreover, the afterward SET-RESET cycles gradually smoothen the sudden resistance drops from 45 to 20 kΩ in Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt memristors (Figure 4f). The continuity in resistance transition simply suggests the tunable resistance states within this range. While the second drop from 20 kΩ to 600 Ω is still abrupt even after ten SET–RESET cycles, such difference further confirms the diverse electrical responses of different sub-filaments. The resistance transition from 45 to 20 kΩ indicates a construction of the first sub-filament (f_1) that contains consecutively tunable states within the 25 kΩ tuning range. The other transition ranging from 20 kΩ to 600 Ω reflects the formation of the second sub-filament (f_2) with merely low resistance (600 Ω) and high resistance (20 kΩ) states. Hence, it is reasonable to assume that f_1 is the filament section ranging from top Pt electrode to the middle Pt islands in the switching layer for the fine adjustment (Pt/Ta/Al_2O_3/Pt sub-memristor). Meanwhile, there are only high and low resistance states in f_2, this sub-filament section plays a coarse adjustment role which is consistent with filament section from middle Pt islands to the

bottom Pt electrode ($Pt/TiO_x/Al_2O_{3-x}/Pt$ sub-memristor). It has been discussed earlier that $Pt/TiO_x/Al_2O_{3-x}/Pt$ sub-memristors require larger voltage and current to be switched ON compared to $Pt/Ta/Al_2O_3/Pt$ sub-memristors. Such observation also coincides with the fact that the voltage and current thresholds of f_2 are higher than f_1. The resistance tuning of f_1 should not affect the internal resistance state of f_2 if the applied current and voltage are less than the thresholds of f_2. It is worth noting that above sub-filaments arrangement is corresponding to the actual dynamic range of $Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt$ memristor. The overall tuning performance of the memristor can be roughly calculated as a resistance summation of f_1 (0–25 kΩ) and f_2 (600 Ω or 20 kΩ). When sub-filament f_2 is kept at low resistance (600 Ω) state, the dynamic range of the entire memristor can be estimated between 600 Ω and 25 kΩ. This range almost matches the LRDR (600 Ω to 19 kΩ). Once f_2 is maintain at high resistance (20 kΩ) state, the resultant tuning range (20–45 kΩ) is also close to HRDR (19–50 kΩ). Here, the slight mismatch between calculated tuning ranges and real tuning range (LRDR and HRDR) can be attributed to the RESET process variation because the device may be reset to a slightly different resistance after each SET–RESET cycle.

4. Conclusion

In summary, we have proposed and experimentally demonstrated $Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt$ memristors with a hybrid tuning mechanism of sub-filaments for the improvement of analog switching performance. By deploying Pt islands into Al_2O_3 switching layer, an entire filamentary channel can be divided into two sub-filaments. Owing to the different material stacks between two sub-filaments, their correlated properties are completely inconsistent. The sub-filament ranging from top Pt electrode to Pt island exhibits continuously tunable resistance range and is considered as a fine resistance adjustment for the overall tuning range. The other sub-filament that connects the Pt island and Pt bottom electrode is responsible for a coarse adjustment because it only possesses high and low resistance states. Compared to $Pt/Ta/Al_2O_3/Pt$ memristor whose dynamic range is from 600 Ω to 8 kΩ, the overall dynamic range is significantly extended (600 Ω to 50 kΩ) in $Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt$ memristors. The coexistence of sub-filaments is confirmed by investigating the resistance evolutions of switching processes. Not only a broader dynamic range is achieved in $Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt$ memristor, but the total amount of stable multilevel states is also increased. In particular, the improvement of dynamic range and multilevel states would be beneficial to the energy efficiency of memristors as well. Our study demonstrates a new method to improve the analog switching performance of memristors, we anticipate this method can be used to enrich the applications of memristive devices for analog computing.

5. Experimental Section

Device Fabrication: The $Pt/Ta/Al_2O_3/Pt/Al_2O_{3-x}/TiO_y/Al_2O_{3-x}/Pt$ memristor was fabricated on a Si wafer with 300 nm SiO_2 film. To fabricate the bottom electrode, a layer of photoresist (AZ 5214, 3000 rpm spin coating for 1 min and baking at 118 °C for 2 min) was coated on the substrate and cured by UV light exposure (54.3 mJ cm^{-2}) under a photomask. Then the sample was immersed in the developer solution (AZ 400K Developer) for 1 min. 2 nm Ti (adhesion layer) and 20 nm Pt (bottom electrode) were deposited on the photoresist by e-beam evaporator (Kurt J. Lesker E-Beam Evaporator) at a growth rate of 0.5 Å s^{-1}. Afterward, a lift-off process was performed on the sample to remove residual photoresist using ultrasonic vibration. The bottom electrode was then covered by 8 nm Al_2O_3 grown by ALD process (Veeco Thermal ALD) under 80 °C. Above 8 nm Al_2O_3 layer, 2 nm Ti, 4nm Al_2O_3, 1 nm Pt, and 4 nm Al_2O_3 were deposited alternatively by e-beam evaporator and ALD. In the end, 8 nm Ta and 20 nm Pt top electrode was patterned by a second photolithography, e-beam evaporator and lift-off process through the same recipe we used to fabricate the top electrode.

Characterization: The optical microscope image was taken using a Nikon Eclipse LV150N microscope. DC electrical characterizations, multilevel resistance state measurements, resistance evolution measurements, retention test, and switching endurance test were all carried out with the Keithley 4200A-SCS parameter analyzer system. In the multilevel states measurements and resistance evolution measurements, the devices were programmed to different resistance states by current pulses (130 ms), and the resistance was read at 100 mV. For the calculation of programmable states, the memristor was tuned to a conductance state and then measured its conductance states for 500 times. The standard deviation σ of these 500 conductance values was calculated to indicate the standard deviation of setting the memristor to an exact conductance state. The number of states could be calculated using the conductance tuning range divided by twice of standard deviation ($N = \frac{conductance\ tuning\ range}{2\sigma}$). For the retention test, the devices were programmed to different resistance states, then reading pulses with 100 mV were sent to the devices every 10 s to measure the conductance and the total test time was 1200 s. In the switching endurance test, the devices were switched between LCS, MCS, and HCS continuously for 300 cycles. The voltage pulse measurement was carried out with Keysight B1500A, the devices were programmed to different conductance states by 500 ns or 100 ns voltage pulses and their conductance was measured after each pulse under 100 mV.

Computational Details: The electric field distribution within Al_2O_3 switching layer with a Pt island was investigated by Comsol Multiphysics, the Electrostatics Model was adopted for the computation. The thickness of switching layer was defined as 16 nm and the radius of Pt island was assigned to be 1 nm. The material of the switching layer was set to Al_2O_3, and the metal material of island was set to Pt (Al_2O_3 and Pt materials chosen from Comsol Multiphysics Materials Library). A 1 V bias was applied to the top electrode and the bottom electrode was set to ground, the calculated electric field within the switching layer is shown in Figure 1b.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The fabrications were performed at the Keck Photonics Center at the University of Southern California. This research was based upon work supported in part by the Office of the Director of National Intelligence (ODNI), Intelligence Advanced Research Projects Activity (IARPA), via 2021–210900005. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies, either expressed or implied, of ODNI, IARPA, or the U.S. Government. The U.S. Government is authorized to reproduce and distribute reprints for governmental purposes notwithstanding any copyright annotation therein. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the authors, and do

not necessarily reflect the views of AFRL or its contractors. This work was partially funded under AFRL's Conduction Channel Engineering in Memristor for Synapse contract, which was started in June, 2019 and continued through October, 2022 (Grant Number FA-8750-19-1-0503).

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

memristive devices, memristors, ReRAM, dynamic ranges, analog switching

Received: March 22, 2023
Revised: April 27, 2023
Published online:

[1] D. B. Strukov, G. S. Snider, D. R. Stewart, R. S. Williams, *Nature* **2008**, *453*, 80.
[2] J. J. Yang, D. B. Strukov, D. R. Stewart, *Nat. Nanotechnol.* **2013**, *8*, 13.
[3] J. J. Yang, M. D. Pickett, X. Li, D. A. Ohlberg, D. R. Stewart, R. S. Williams, *Nat. Nanotechnol.* **2008**, *3*, 429.
[4] S. Pi, C. Li, H. Jiang, W. Xia, H. Xin, J. J. Yang, Q. Xia, *Nat. Nanotechnol.* **2019**, *14*, 35.
[5] R. Waser, M. Aono, In *Nanoscience And Technology: A Collection of Reviews from Nature Journals* (Ed: P. Rodgers), World Scientific, Singapore **2010**, pp. 158-165.
[6] E. Linn, R. Rosezin, C. Kügeler, R. Waser, *Nat. Mater.* **2010**, *9*, 403.
[7] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, W. Lu, *Nano Lett.* **2010**, *10*, 1297.
[8] M. A. Zidan, J. P. Strachan, W. D. Lu, *Nat. Electron.* **2018**, *1*, 22.
[9] A. Thomas, *J. Phys. D: Appl. Phys.* **2013**, *46*, 093001.
[10] J. Tang, F. Yuan, X. Shen, Z. Wang, M. Rao, Y. He, Y. Sun, X. Li, W. Zhang, Y. Li, *Adv. Mater.* **2019**, *31*, 1902761.
[11] A. A. Bessonov, M. N. Kirikova, D. I. Petukhov, M. Allen, T. Ryhänen, M. J. Bailey, *Nat. Mater.* **2015**, *14*, 199.
[12] S. G. Kim, J. S. Han, H. Kim, S. Y. Kim, H. W. Jang, *Adv. Mater. Technol.* **2018**, *3*, 1800457.
[13] R. Waser, R. Dittmann, G. Staikov, K. Szot, *Adv. Mater.* **2009**, *21*, 2632.
[14] A. Wedig, M. Luebben, D.-Y. Cho, M. Moors, K. Skaja, V. Rana, T. Hasegawa, K. K. Adepalli, B. Yildiz, R. Waser, *Nat. Nanotechnol.* **2016**, *11*, 67.
[15] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, R. S. Williams, *Nature* **2010**, *464*, 873.
[16] Z. Wang, S. Joshi, S. E. Savel'ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li, *Nat. Mater.* **2017**, *16*, 101.
[17] J. J. Yang, F. Miao, M. D. Pickett, D. A. Ohlberg, D. R. Stewart, C. N. Lau, R. S. Williams, *Nanotechnology* **2009**, *20*, 215201.
[18] M. D. Pickett, D. B. Strukov, J. L. Borghetti, J. J. Yang, G. S. Snider, D. R. Stewart, R. S. Williams, *J. Appl. Phys.* **2009**, *106*, 074508.
[19] B. Choi, D. Jeong, S. Kim, C. Rohde, S. Choi, J. Oh, H. Kim, C. Hwang, K. Szot, R. J. Waser, *J. Appl. Phys.* **2005**, *98*, 033715.
[20] F. Miao, J. P. Strachan, J. J. Yang, M. X. Zhang, I. Goldfarb, A. C. Torrezan, P. Eschbach, R. D. Kelley, G. Medeiros-Ribeiro, R. S. Williams, *Adv. Mater.* **2011**, *23*, 5633.
[21] J. Y. Chen, C. W. Huang, C. H. Chiu, Y. T. Huang, W. W. Wu, *Adv. Mater.* **2015**, *27*, 5028.
[22] C. Li, M. Hu, Y. Li, H. Jiang, N. Ge, E. Montgomery, J. Zhang, W. Song, N. Dávila, C. E. Graves, *Nat. Electron.* **2018**, *1*, 52.
[23] M. Hu, C. E. Graves, C. Li, Y. Li, N. Ge, E. Montgomery, N. Davila, H. Jiang, R. S. Williams, J. J. Yang, *Adv. Mater.* **2018**, *30*, 1705914.
[24] Q. Xia, J. J. Yang, *Nat. Mater.* **2019**, *18*, 309.
[25] D. S. Jeong, K. M. Kim, S. Kim, B. J. Choi, C. S. Hwang, *Adv. Electron. Mater.* **2016**, *2*, 1600090.
[26] Y. Yang, W. Lu, *Nanoscale* **2013**, *5*, 10076.
[27] W. Huh, D. Lee, C. H. Lee, *Adv. Mater.* **2020**, *32*, 2002092.
[28] B. Chen, H. Yang, B. Song, D. Meng, X. Yan, Y. Li, Y. Wang, P. Hu, T.-H. Ou, M. J. Barnell, *Sci. Robot.* **2020**, *5*, eabb6938.
[29] Y. Zhang, Z. Wang, J. Zhu, Y. Yang, M. Rao, W. Song, Y. Zhuo, X. Zhang, M. Cui, L. Shen, *Appl. Phys. Rev.* **2020**, *7*, 011308.
[30] Y. Li, Z. Wang, R. Midya, Q. Xia, J. J. Yang, *J. Phys. D: Appl. Phys.* **2018**, *51*, 503002.
[31] S. Choi, J. Yang, G. Wang, *Adv. Mater.* **2020**, *32*, 2004659.
[32] S. Xu, B. Evans, D. I. Flynn, C. J. En, *Thin Solid Films* **1994**, *238*, 54.
[33] S. Kim, S. Choi, W. Lu, *ACS Nano* **2014**, *8*, 2369.
[34] Y. Jeong, S. Kim, W. D. Lu, *Appl. Phys. Lett.* **2015**, *107*, 173105.
[35] B. Song, Z. Jiang, Z. Liu, Y. Wang, F. Liu, S. B. Cronin, H. Yang, D. Meng, B. Chen, P. Hu, *ACS Nano* **2020**, *14*, 14769.
[36] W. Fang, P. Hu, Z. Wu, Y. Xiao, Y. Sui, D. Pan, G. Su, M. Zhu, P. Zhan, F. Liu, W. Wu, *Nanotechnology* **2021**, *32*, 355301.
[37] M. Li, Q. Ma, W. Zi, X. Liu, X. Zhu, S. Liu, *Sci. Adv.* **2015**, *1*, e1400268.
[38] M. Wang, S. Cai, C. Pan, C. Wang, X. Lian, Y. Zhuo, K. Xu, T. Cao, X. Pan, B. Wang, *Nat. Electron.* **2018**, *1*, 130.
[39] H. Yang, B. Chen, B. Song, D. Meng, S. Tiwari, A. Krishnamoorthy, X. Yan, Z. Liu, Y. Wang, P. Hu, T.-H. Ou, P. Branicio, R. Kalia, A. Nakano, P. Vashishta, F. Liu, H. Wang, W. Wu, *ACS Appl. Electron. Mater.* **2020**, *2*, 1529.
[40] P. Bousoulas, I. Michelakaki, D. Tsoukalas, *J. Appl. Phys.* **2014**, *115*, 034516.
[41] Y. N. Joglekar, S. J. Wolf, *Eur. J. Phys.* **2009**, *30*, 661.
[42] A. Rahmel, P. Spencer, *Oxid. Met.* **1991**, *35*, 53.
[43] L. Alekseeva, T. Nabatame, T. Chikyow, A. Petrov, *Jpn. J. Appl. Phys.* **2016**, *55*, 08PB02.
[44] J. G. Speight, *Lange's Handbook of Chemistry*, McGraw-hill, New York, **2005**.
[45] Y. Li, K.-S. Yin, M.-Y. Zhang, L. Cheng, K. Lu, S.-B. Long, Y. Zhou, Z. Wang, K.-H. Xue, M. Liu, *Appl. Phys. Lett.* **2017**, *111*, 213505.